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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
REQUEST FOR FILING NATIONAL PATENT APPLICATION
under 35 USC 111(a) and Rule 53(b) WITH SIGNED DECLARATION

PATENT APPLICATION

Asst. Commissioner for Patents
BOX PATENT APPLICATION
Washington, D.C. 20231

NONPROVISIONAL

Sir:

Enclosed is the patent application of
Inventor: William J. Dally
Title: Streaming Memory System

(Our Deposit Account No. 03-3975)

Our Order No.	81013	259709
	Client #	Matter #
Atty. Docket	259709	S97-245
	TMC#	Client Ref

including:

Date: September 13, 1999

1. [X] Specification: **15** pages
2. [ ] Specification in non-English
3. [X] Declaration (unsigned)
4. [X] Drawings: **2** sheet(s) [X] informal [ ] formal
5. [ ] An Assignment and cover sheet. Please return the recorded Assignment to the undersigned.
6. [X] **2** Verified Statements establishing "small entity" status under Rules 9 & 27.

THE FOLLOWING FILING FEE IS BASED ON CLAIMS AS FILED LESS ANY ABOVE CANCELLED

7. Basic Filing Fee.....				$760/$380	$ 380.00	101/201
8. Total Claims:	19	minus 20 =	0	x $18/$9 =	+	103/203
9. Independent Claims:	2	minus 3 =	0	x $78/$39 =	+	102/202
10. TOTAL FILING FEE ENCLOSED =					**$ 380.00**	
11. If "assignment" box is X'd, add recording fee.....				+ $40/$40	+	581
TOTAL FEE ENCLOSED:					**$ 380.00**	

CHARGE STATEMENT: The Commissioner is hereby authorized to charge any missing or insufficient fees required under Rules 16-18 relative to this application and the resulting Official document under Rule 20, or credit any overpayment, to our Account/Order No. above, for which purpose a duplicate copy of this sheet is enclosed. This CHARGE STATEMENT does not authorize charge of the issue fee until/unless an issue fee transmittal form is filed.

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Gayle D. Peterson

Gayle D. Peterson

Applicant: **William J. DALLY**
Serial No: **Unassigned**

Atty Docket No. **81013/259709**
Filed: **Herewith**

Title: ***Streaming Memory System***

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
37 CFR 1.9(f) and 1.27(d)--NONPROFIT ORGANIZATION

I hereby declare that I am an official empowered to act on behalf of the following nonprofit organization:

Name of Organization: **Massachusetts Institute of Technology**
Address: **77 Massachusetts Avenue, Cambridge, MA 02142**
Type of Organization: **University**

I declare that the above identified nonprofit organization qualifies as a nonprofit organization as defined in 37 CFR 1.9(e), for purposes of paying reduced fees under 41(a) or (b) of Title 35, U.S. Code, with regard to the invention entitled ***Streaming Memory System*** by inventor **William J. Dally**, described in [X] the specification filed herewith.

I declare that rights under contract or law have been conveyed to and remain with the nonprofit organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e). *Note: separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

Name: _____
Address: _____
[ ] individual [ ] small business concern [ ] nonprofit organization

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28(b)).

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 1001 of Title 18 of the U.S. Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of person signing: Jarmila Z. Hrbek
Title in Organization: Patent Administrator and Office Manager
Address of person signing: Technology Licensing Office
77 Massachusetts Avenue
Cambridge, MA 02139

Client Ref. **MIT-8142**

Signature: Jarmila Z Hrbek Date: September 1, 1999

Applicant: William J. DALLY
Serial No: Unassigned

Atty Docket No. 81013/259709
Filed: Herewith

Title: *Streaming Memory System*

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS
37 CFR 1.9(f) and 1.27(d)--NONPROFIT ORGANIZATION

I hereby declare that I am an official empowered to act on behalf of the following nonprofit organization:

Name of Organization: **The Board of Trustees of the Leland Stanford Junior University**
Address: **Stanford, California 94305-6225**
Type of Organization: **University**

I declare that the above identified nonprofit organization qualifies as a nonprofit organization as defined in 37 CFR 1.9(e), for purposes of paying reduced fees under 41(a) or (b) of Title 35, U.S. Code, with regard to the invention entitled ***Streaming Memory System*** by inventor **William J. Dally**, described in [X] the specification filed herewith.

I declare that rights under contract or law have been conveyed to and remain with the nonprofit organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9(d) or by any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e). *Note: separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

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Address: _____

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I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further, that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 1001 of Title 18 of the U.S. Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Name of person signing: Katharine Ku
Title in Organization: Director, Office of Technology Licensing
Address of person signing: Stanford University, Stanford, California 94305

Client Ref. S97-245

Signature: Katharine Ku Date: September 13, 1999

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STREAMING MEMORY SYSTEM

BACKGROUND OF THE INVENTION

Priority is claimed under 35 U.S.C. 119(e) based on provisional application no. 60/100,147 filed September 14, 1998.

1. Field of the Invention

The present invention relates to a memory control and, more particularly, a memory control system that allows faster access to memory cells.

2. Description of Related Art

Modern computer systems use well known dynamic memory chips that are arranged as a matrix of rows and columns. FIGS. 1-3 illustrates such dynamic memory chips. As illustrated in FIG. 1, the various memory cells are disbursed within different banks, such as banks 1-8 illustrated in FIG. 1. FIG. 2 illustrates certain of the components within a given bank of the memory. As is known, associated with the bank will be a row decoder 22, a column decoder 24, a memory array 26, a **sense** amplifier 28, and column selection circuitry 30, also referred to herein as I/O circuitry.

A portion of the memory array 26 is further illustrated in FIG. 3, as shown, a plurality of memory cells 30 are attached to particular rows 32, (also known as word lines) and columns 34 (also known as bitlines).

Operation of memories as described above is well known, for example that an address will be input to the memory array, a memory cell associated with the input address will be accessed, and the data stored in that memory cell can be read out. Similarly, if data needs to be written into the memory array, the data will have an associated address, and that address will be used to store the data into the memory cell associated with that particular address.

Memory chips as described above also use techniques in order to increase their speed and efficiency. Using conventional techniques, such chips can access a word of data in a different column of a pre-selected row in a very efficient manner (typically one word per cycle) but access to a word in a different (non-selected) row is relatively slow (typically ten cycles). Furthermore, since these chips are divided into banks as mentioned previously, which each include separate row/column matrices, as illustrated in FIG. 3, this allows for a row access to be performed on one bank while column accesses are being made to a different bank. While such operation improves efficiency somewhat, improvements are still needed.

Particularly, conventional memory systems process memory operations in the order they are received. If they receive addresses in the same row as the previous address, then a column access is performed. Otherwise, a row access is performed. While this mode of operation yields adequate performance for access patterns with significant spacial locality, performances are degraded by almost 90% for unstructured address streams. Such unstructured address streams are typically of indirect vector or stream references.

Accordingly, an improved streaming memory system is needed that allows for improved performance in accessing unstructured address streams.

BRIEF SUMMARY OF THE INVENTION

It is an object of the present invention to increase memory performance for access to unstructured address streams.

Another object of the present invention to complete memory access operations in an order different from the order that such memory access operations were requested.

In order to achieve the above object of the inventions, among others, the present invention is a memory system that receives addresses corresponding to data in an order. The memory system includes an address buffer that receives addresses in the order provided by a computer system, a memory array, a control circuit that presents addresses to the memory array in an order different than the order in which they were received by the address buffer; and a read buffer that receives data read out from the memory array.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1-3 illustrate a conventional dynamic random access memory device.

FIG. 4 illustrates a streaming memory system according to the present invention.

DETAILED DESCRIPTION OF PRESENTLY PREFERRED EMBODIMENTS

FIG. 4 illustrates the streaming memory system according to the present invention. The invention includes an address buffer 52, memory 54, a read buffer 56, and

a schedule/control circuit 58, each of which are described in further detail hereinafter. While in the presently preferred embodiment, the memory 54 is a discrete semiconductor circuit chip, it is contemplated that the streaming memory system according to the present invention can also be implemented on a single integrated chip.

With reference to FIG. 4, the address buffer 52 inputs addresses that will be used by the memory 54 to access certain particular memory cells during a read or write operation. The address buffer 52 must be large enough to store addresses for a predetermined number of memory accesses that have been provided by the overall computer system 60, such as four, eight or more.

Whereas in conventional systems addresses are supplied to the memory device and operated upon in the supplied order, the present invention includes an address buffer 52 which receive and queues a number of addresses, such as 8 different addresses. The present invention has the capability of advantageously operating upon these addresses in an order different from that received by the address buffer 52, which helps promote efficient operation as has been mentioned and will be described further hereinafter. Because the addresses will be operated upon in an order different than that received, the present invention also includes a read buffer 56, which stores the data that is read out from the memory device 54. This allows, therefore, the data that is read out to be stored and subsequently transmitted from the read buffer 56 to the computer system 60 in the same order as the order in which the addresses were received by the address buffer 52 from the computer system 60, for those addresses corresponding to read operations. The schedule/control circuit 58 controls the operation of re-ordering the addressing, as will now be further described. It should be noted, however, that the operations that are

conventionally required in order to access a memory device are not described in detail. In fact, such conventional operations will differ depending upon the type of memory device that exists, such as conventional dynamic random access memories, synchronous dynamic random access memories, or rambus dynamic random access memories, as well as other types of memories that are accessed as one or more banks of rows and columns.

On initiation of a new cycle, a new address is input to the address buffer 52 and the comparison of addresses in the address buffer 52 with the address of the active row in the previous cycle is made using a comparator that compares the row address of each address with the row address of the currently active row. If one of more of the addresses in the address buffer 52 correspond to an address associated with the active row from the previous cycle (also termed currently active row), the schedule/control circuit 58 will initiate those control signals required to perform column addressing of the oldest address in the address buffer 52 that corresponds to the active row using a priority encoder that selects the first address entered into the address buffer that is contained in the currently active row. That address, therefore, will be operated upon during that cycle be input into memory 54 so that the memory cell associated with that address can be accessed. Thus, the comparator and priority encoder, which are implemented preferably using hardwired logic that make up the schedule/control circuit 58, operate every cycle in parallel to select an access to be run. Each cycle the logic scans the addresses in the address buffer 52 to find one (if any) that is to an active row and selects this address for a column access.

If a simultaneous row access is also possible, the logic in the schedule/control circuit 58 also scans the addresses to find one for which a row access

would be profitable, one for which there are no more addresses to the active row in its bank and (optionally) for which there are several other addresses in the same row queued. Thus, for certain memory devices, while column addressing of an address is performed, the schedule/control circuit 58 can also initiate row addressing of a row in a bank other than the currently active row bank. For instance, if column addressing of an address associated with the active row is accessing data in bank 1, the schedule/control circuit 58 may initiate row addressing for a row within bank 6, since bank 6 does not currently contain an active row, so that in a subsequent cycle column addressing of that row can take place. Thus, according to the present invention, row access latency can be hidden under column accesses to other banks, thus improving efficiency of this system.

Once a row access is initiated, the schedule/control circuit 58 will also initiate subsequent control operations, depending on whether a read or a write operation was to take place.

If a write operation takes place, the associated data is written into the addressed memory cell location.

If a read operation takes place, the schedule/control circuit will cause the read out of data from the addressed memory cell location, and storage of that data into a read buffer 56 so that the data can read out of the read buffer 56 in the order that the read addresses were initially received into the address buffer 52. More particularly, in a read operation, the read buffer 56 is indexed by a pair of pointers in a manner such as that used to reorder instructions in processors that allow out of order execution. As each read access is inserted into the address buffer 52, the next sequential location in the read buffer 56 is identified by a read-tail pointer, reserved for this access, and marked pending. The

value of the read-tail pointer is queued with the address in the address buffer 52 to record the location assigned and the read-tail pointer is incremented modulo the size of the read buffer 56. When the queued read access is actually performed, the data read is inserted into the read buffer 56 location reserved for this access using the pointer queued with the address in the address buffer 52 and this location is marked full.

A read-head pointer is used to remove data from the read buffer 56. On reset the read-head and read-tail pointer both point to the same location and that location is marked empty. As read accesses arrive, the read-tail pointer is incremented by the schedule/control circuit 58 and locations are marked pending to allocate sequential read buffer 56 locations to these sequential accesses. Finally, as read accesses are performed, some of these pending locations are filled.

Whenever the location identified by the read-head pointer is marked full, the value in that location is output, the location marked empty, and the read-head pointer incremented modulo the size of the read buffer 56. Because the read-data for the accesses is output in the same order that the read addresses arrived, ordering, read order is preserved even though memory accesses are performed out of order. The read buffer 56 in effect reorders the out of order memory accesses.

Ordering is also important in a memory system, and the present invention allows for completion of memory write operations out of order with operations that read or write other memory rows because these operations are guaranteed not to be of the same address. The schedule/control circuit 58 always performs accesses in the same row in the original requested order, thus preserving the original order for two writes to the same location or a read and a write to a given location. The present system preserves the

ordering of write operations and the relative ordering of reads and writes by always scanning for accesses to an active row in the order that accesses arrived. Thus, an 'older' access to a given row, and hence a given location, will always occur before a later access to the same row, and hence same location. Only accesses to distinct rows and hence distinct locations are reordered. Thus, read before write or write before read hazards are not a problem with the schedule/control circuit 58 re-ordering.

In a preferred implementation of the present invention, the address buffer and the read buffer are partitioned so that addresses and data for each of the separate banks are buffered separately. Thus, the schedule/control circuit can access the partitioned buffer associated with a currently active bank, perform an equality comparison on a those address bits necessary to determine if another address in the partitioned buffer corresponds to the currently active row in the currently active bank in order to determine whether to perform fast column addressing for the currently active bank using the another address, or instead initiate addressing of another bank in the manner previously described such that row addressing of another bank is performed while the fast column addressing of the bank that previously had an associated active row is ongoing.

The present invention also contemplates initiating access of multiple rows in different banks at the same time.

Although the present invention has been described in detail with reference to the specific embodiments and examples provided herein, those skilled in the art will realize that various modifications and/or substitutions could be made to such specific

examples while remaining within the spirit and scope of the invention as set forth in the appended claims.

WHAT IS CLAIMED IS:

1. A memory system that receives addresses corresponding to data in an order comprising:

an address buffer that receives addresses in said order;

a memory array;

a control circuit that presents addresses to the memory array in an order different than the order in which they were received by the address buffer; and

a read buffer, that receives data read out from the memory array.

2. A memory system according to claim 1 wherein said control circuit causes the read buffer to read out data from the read buffer in said order with respect to read requests.

3. A memory system according to claim 1 wherein the control circuit performs multiple accesses in sequential cycles to a given row in the memory in the order in which the addresses corresponding to the given row were received.

4. A memory system according to claim 1 wherein the memory array is partitioned into a plurality of banks, and the control circuit performs multiple accesses in sequential cycles to an active row of a given bank before activating a different row of the given bank.

5. A memory system according to claim 1 wherein the memory array is partitioned into a plurality of banks, and the control circuit performs multiple accesses in sequential cycles to an active row of a given bank before activating a different bank.

6. A memory system according to claim 1 wherein the memory array is partitioned into a plurality of banks, and the control circuit performs a row access to a currently inactive bank when another bank contains a currently active row.

7. A memory system according to claim 1 wherein the memory array is partitioned into a plurality of banks and the address buffer is partitioned into a separate address buffer for each bank.

8. A memory system according to claim 1 wherein said control circuit comprises:

a comparator for each address capable of being stored in the address buffer which compares the row address of each address with the row address of the currently active row; and

a priority encoder that selects the first address entered into the address buffer that is contained in the currently active row.

9. A memory system according to claim 1 wherein, associated with the read buffer is a head pointer and a tail pointer to assist in tracking the order sequence of read access requests, and a buffer array containing a status flag for each read access request having an associated address currently stored in the address buffer.

10. A memory system according to claim 1 wherein, during each of a plurality of sequential cycles, the address buffer inputs a new address and the control circuit compares the new address to the address of the currently active row.

11. A memory system according to claim 7 wherein, during each of a plurality of sequential cycles, the address buffer inputs a new address and the control circuit compares the new address to the address of the currently active row if the currently active row is in the same bank as the new address.

12. A memory system according to claim 11 wherein, if the address buffer inputs the new address and the new address does not correspond to the same bank as the address of the currently active row, the control circuit does not perform a comparison of the new address to the address of the currently active row.

13. Method of accessing memory comprising the steps of:

receiving a sequential plurality of memory access requests in the form of an address inputs;

buffering the plurality of address inputs;

initiating an out of order memory access request to a memory array for one of the sequential plurality of memory access requests such that one of the plurality of address inputs is requested in an order different than the order in which the one address was received; and

buffering read results of those memory access requests corresponding to read operations.

14. A method according to claim 13 wherein said step of initiating initiates the out of order memory access request initiates said request to an address having a row corresponding to a currently active row.

15. A method according to claim 13 wherein the buffered read results are read out in the in the order that the original read requests were made.

16. A method according to claim 13 wherein multiple accesses in sequential cycles to a given row in the memory array are made in the order in which the addresses. corresponding to the given row were received.

17. A method according to claim 13 wherein a plurality of row accesses are performed out of order to a currently active row before another row is made currently active.

18. A method according to claim 13 wherein the memory array is partitioned into a plurality of banks, and a row access is performed on a row of a currently inactive bank when another bank contains a currently active row.

19. A method according to claim 13 wherein the step of buffering read results includes setting a read-tail pointer to identify a next sequential location of a buffer and setting a read-head pointer to remove data from the buffer.

ABSTRACT OF THE DISCLOSURE

The present invention is a memory system that receives addresses corresponding to data in a sequential order. The memory system includes an address buffer that receives addresses in the order provided by a computer system, a memory array, a control circuit that presents addresses to the memory array in an order different than the order in which they were received by the address buffer; and a read buffer that receives data read out from the memory array.

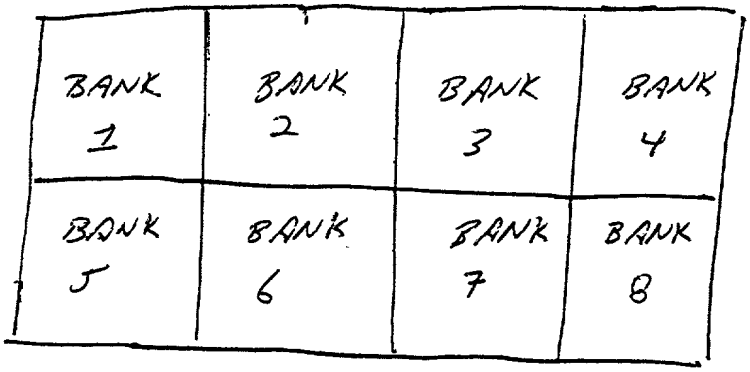

FIG 1 (Prior Art)

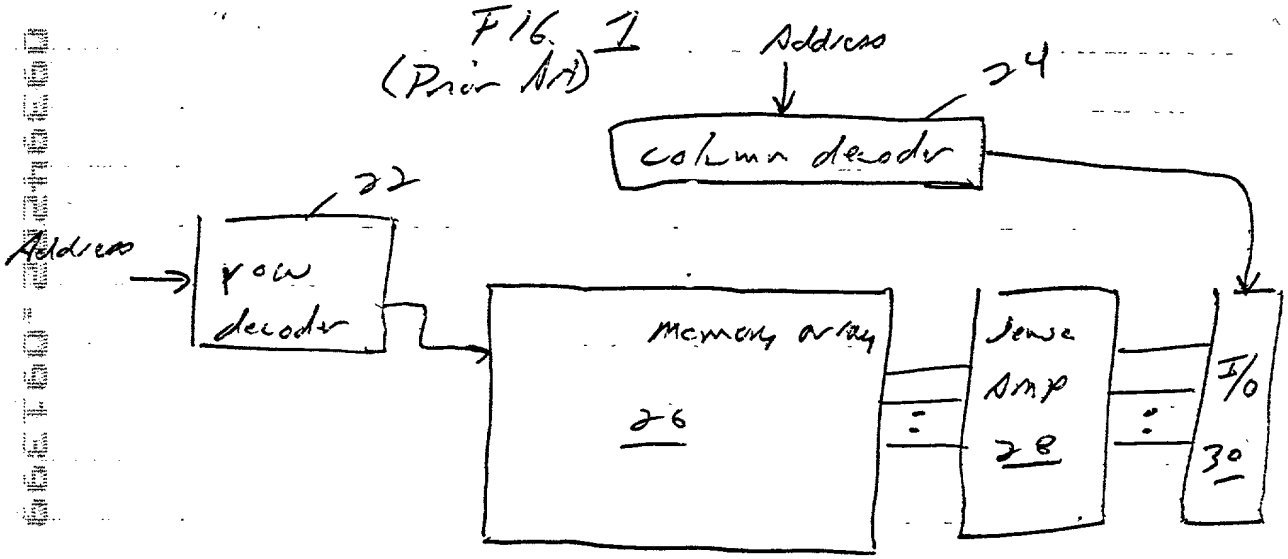

Fig 2 (Prior Art)

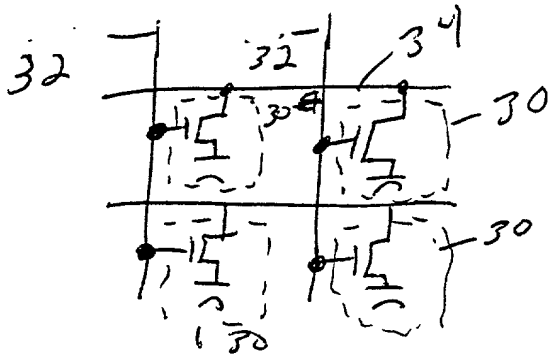

Fig 3 (Prior Art)

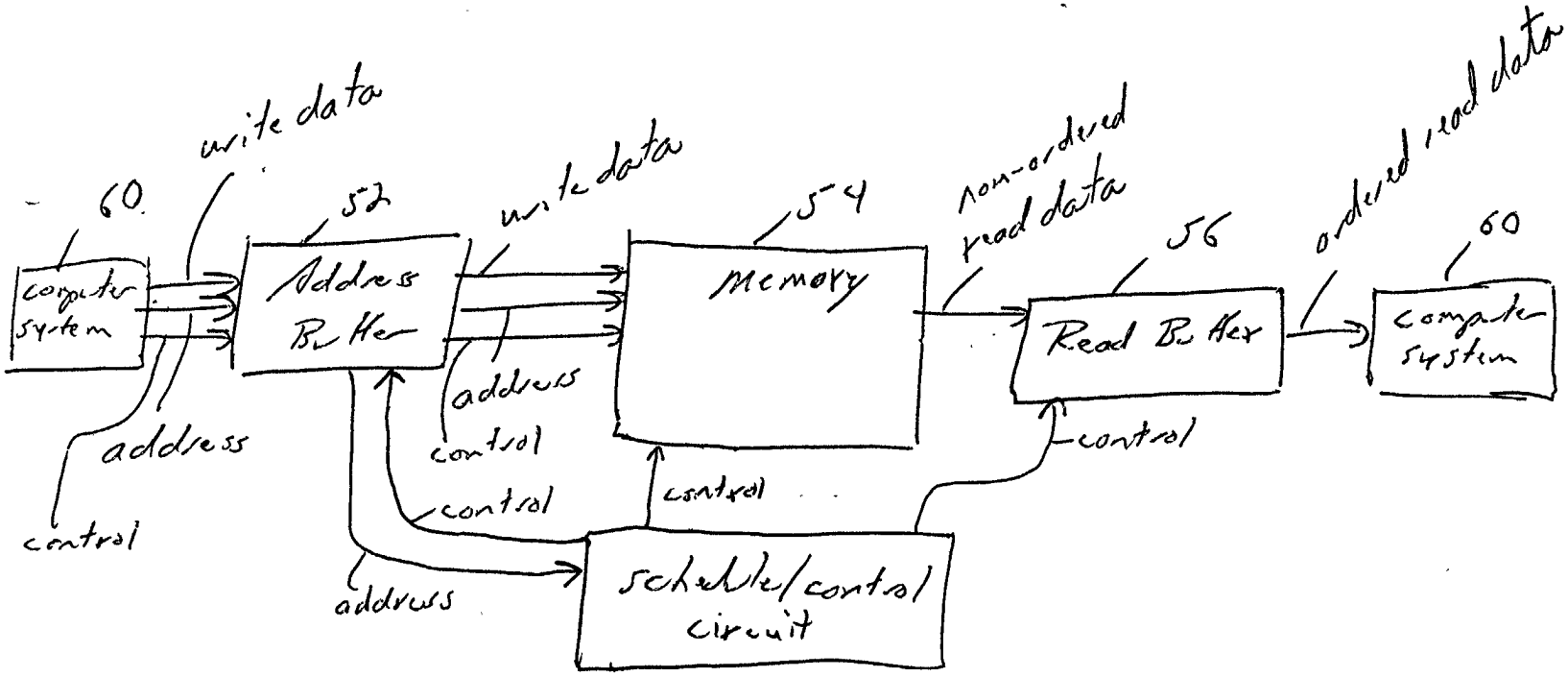

Fig 4

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled, **Streaming Memory System**, the specification of which is attached hereto, bearing Atty Docket No. 81013/259709.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56. I hereby claim foreign priority benefits under 35 U.S.C. 119/365 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate filed by me or my assignee disclosing the subject matter claimed in this application and having a filing date (1) before that of the application on which priority is claimed, or (2) if no priority claimed, before the filing date of this application: PRIOR FOREIGN APPLICATION(S):

Number	Country	Day/MONTH/Year Filed	Date first Laid-open or Published:	Date Patented or Granted:	Priority Claimed? Yes [ ] No [ ]

I hereby claim domestic priority benefit under 35 U.S.C. 119/120/365 of the indicated United States applications listed below and PCT international applications listed above or below and, if this is a continuation-in-part (CIP) application, insofar as the subject matter disclosed and claimed in this application is in addition to that disclosed in such prior applications, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56 which became available between the filing date of each such prior application and the national or PCT international filing date of this application: PRIOR U.S. PROVISIONAL, NONPROVISIONAL AND/OR PCT APPLICATIONS:

Application No.:	Day/MONTH/Year Filed:	Status (pending, abandoned, patented)	Priority Claimed?
60/100,147	**14/09/98**	**pending**	Yes [X] No [ ]

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

I hereby appoint Pillsbury Madison & Sutro LLP, 1100 New York Avenue, N.W., Ninth Floor, East Tower, Washington, D.C. 20005-3918, tel. (650) 233-4776 (to whom all communications are to be directed), and the below-named persons (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent, and I hereby authorize them to delete names of persons no longer with their firm and to act and rely on instructions from and communicate directly with the assignee which first sent this case to them and by which I hereby declare that I have consented after full disclosure to be represented, unless/until I instruct the above Firm in writing to the contrary.

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INVENTOR'S SIGNATURE: _____ Date _____

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Country of Citizenship: **United States of America**